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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,555	03/22/2001	David B. Squires	X-857 US	6451

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EXAMINER	
HUYNH, KIM NGOC	
ART UNIT	**PAPER NUMBER**
2182	5

DATE MAILED: 01/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/815,555	SQUIRES, DAVID B.	
	Examiner	Art Unit	
	Kim Huynh	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 6 and 10-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 6 recites the programmable logic device of claim 1 comprising a processor core, a configurable peripheral device and a bus. The specification does not provide support for such limitation. The specification defines the programmable logic device (CLB) as reference 127 and 128, the specification does not provide any support for the core, the peripheral device and the bus being programmable logic device. The examiner will interpret that the core, peripheral device and bus are implemented (put into practice with) on a FPGA as recited in claim 4.

Claims 10-13 are rejected because they depend from claim 6.

Claim 14 recite the integrated circuit having a user interface and computer display system. The specification fails to support an integrated circuit to include a user

interface or a computer display system. Furthermore, no display system is found in the disclosure.

3. The following rejections are made based on the examiner's best interpretation of the claims in light of the 35 USC 112 rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 4, 5-6 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Akao (US 5,307,464).

Claims 1 and 6, Akao discloses a microcontroller and system for allowing the user to select the peripheral devices (Figs. 1-2 and 10) having a bus, processor core 2, a configurable logic control block 102 coupled to the core, configurable peripheral devices 3-5 wherein the peripheral are logic external to the CPU such as interface circuits, timers, counters, and serial input/output control circuits. Please note the recitation of the configurable logic control block is not limiting.

Claim 4, Akao discloses the peripheral and bus are implemented on a FPGA (see Figs. 15-17 and 20).

Claims 2 and 5, Akao discloses the configurable peripheral devices (peripheral functions) can be of counter, timer, serial communication (UART), ROM, RAM.

As best understood of claim 14 per the 35 USC 112 rejection above, the integrated circuit is implemented on a system which include a user interface and a computer display for selecting the function of the configurable device (see Fig. 10 and col. 2, ll. 10-23).

6. Claims 1, 4, 6 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Basset (US 5,812,867).

Claim 1, Basset discloses an integrated circuit having a bus connecting between a processor core 1, a programmable logic control block (decoders 20-21) and a configurable peripheral device 3.

Claim 4, Basset discloses the configurable peripheral device and bus are implemented on a FPGA (see Fig. 7).

Claims 6 and 14 Basset discloses a system allowing a user to select peripheral devices in a programmable logic device (col. 6, ll. 50-67) having menu system (choice of options, col. 6, ll. 65-67) allowing the user to select one of the plurality of peripheral devices and an integrated circuit as recited in claim 1. Please note Basset discloses the integrated circuit having more than one peripheral device 3 (abstract).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-3, 5, and 10-13 are rejected under 35 U.S.C. 103(a) as being obvious over Basset in view of Mattheis et al. (US 6,085,337), Davidson et al. (US 5,428,748) or applicant's admission (page 4, ll. 4-10).

Claims 2-3, 5, and 10-13, Basset does not specify the type of peripheral devices. however, Mattheis discloses that peripheral such as UART, memory, watchdog timer are typical in microcontroller depending on the product containing in the microcontroller (background, col. 1, ll. 10-18). Davidson discloses peripheral devices such as memory, communication interface are typical to carry out the digital data processing function. This is in line with applicant admission that peripheral such as UART, flash memory controller, interface devices are typical peripheral devices and is not significant. Therefore, it would have been obvious to one having ordinary skill in the art to select any type of peripheral devices in order to enable the configuration of the desired peripherals selected depending on the user's choice and application of the particular microcontroller.

Please note UART with fixed baud rate is of conventional construction such as type NSC 858 chip manufactured by National Semiconductor Corporation or other conventional UART such as Intel 8251 or 8252. It would have been obvious to one having ordinary skill in the art to utilize any of the conventionally available UART chip in order to simplify the design of the microcontroller depending on the type of data transmission required.

As for the selecting of width size and error correction, please note these are properly of memory. The system of Bassett is designed for choosing the desired

option of the peripheral devices (col. 2, ll. 53-64); therefore would have been obvious to one having ordinary skill in the art to modify the system of Basset for the user to select options that is related to the peripheral being connected to the setup system based on the user's need and the operational specification of the peripheral device.

9. Claims 3 are rejected under 35 U.S.C. 103(a) as being obvious over Akao. Akao does not disclose the UART is of fixed baud rate. However, it would have been obvious to one having ordinary skill in the art to implement the UART of any rate depending on the user's application of the microprocessor to carry out the transmitting of data.

10. Claims 2, 5, 7 and 10-13 are rejected under 35 U.S.C. 103(a) as being obvious over Akao in view of Mattheis et al. (US 6,085,337), Davidson et al. (US 5,428,748) or applicant's admission (page 4, ll. 4-10).

Similarly, claims 2, 5, 7, 10-13 are rejected for the same reasoning as discussed above, as for the selecting of width size and error correction, please note these are properly of memory. The system of Bassett is designed for choosing the desired option of the modify the peripheral functions and performance of the appropriate application (col. 2, ll. 10-35); therefore would have been obvious to one having ordinary skill in the art to modify the system of Akao for the user to select options that is related to the peripheral being connected to the setup system based on the user's need and the operational specification of the peripheral device (col. 1, ll. 7-17).

Response to Arguments

11. Applicant's arguments with respect to claims 1,4, and 6 have been considered but are moot in view of the new ground(s) of rejection.

Please note the recitation of the configurable logic control block is not limiting, the limitation is broad and any type of control logic would read on this limitation.

As for the argument that the peripheral devices of Akao are not FPGA, please note the ROM, RAM, and the address register are gate arrays which are programmable and therefore by definition, are FPGA.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703) 308-1678.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Kim Huynh
Primary Examiner
Art Unit 2182

KH
January 22, 2004